AF/2815

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Mostafazadeh et al.

Application No.: 09/625,071

Filed: July 25, 2000

Title: LEAD FRAME CHIP SCALE PACKAGE

Attorney Docket No.:
NSC1P217D2/NS-3877-2

Examiner: Clark, S.

Group: 2815

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on August 1, 2003 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: Lara M. Nelson
Lara M. Nelson

APPEAL BRIEF TRANSMITTAL
(37 CFR 192)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on July 7, 2003. This brief is transmitted in triplicate.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
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☐ Applicant(s) hereby petition for a _____ extension(s) of time to under 37 CFR 1.136.

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extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 500388.

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Appeal Brief fee	$320.00
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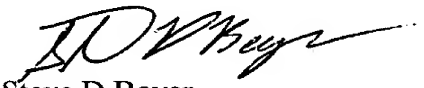
Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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#28 Appeal Brief 8/13/03 aR

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF APPEALS

EX PARTE MOSTAFAZADEH et. al.

Application for Patent

Filed July 25, 2000

Serial No. 09/625,071

FOR:

LEAD FRAME CHIP SCALE PACKAGE

APPEAL BRIEF

CERTIFICATE OF MAILING

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Signed: Lara M. Nelson
Lara M. Nelson

BEYER WEAVER & THOMAS
Attorneys for Applicant

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I. REAL PARTY IN INTEREST

The real party in interest is National Semiconductor Corp., the assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

The undersigned is not aware of any related appeals and/or interferences.

The application is related to U.S. Patent Nos. 6,589,814 and 6,130,473. The '473 patent is currently the subject of a reissue application.

III. STATUS OF THE CLAIMS

Claims 11-13, 15-33 and 38-44 are pending and subject to this appeal. Each of the pending claims stands rejected under 35 USC §103. Claims 11, 13, 18, 26 and 38 also stand rejected under 35 USC 112, first paragraph.

Claims 1-10, 14, and 34-37 have all been cancelled. It is noted that the final Office Action Summary dated May 6, 2003 inadvertently identifies claims 34 and 36 as rejected and those claims are also identified on the notice of appeal. However, both claims were cancelled in the amendment Mailed January 8th, 2003 and are not subject to this appeal.

All of the pending claims stand rejected and are subject to this appeal.

IV. STATUS OF AMENDMENTS

The applicants filed a Request for Reconsideration after the final rejection by the Examiner dated May 6, 2003. The Request for Reconsideration was mailed on June 4, 2003 and did not contain any amendments. In an advisory action dated June 20, 2003, the Examiner indicated that the Request for Reconsideration did not put the case in condition for allowance.

V. SUMMARY OF INVENTIONS

The claimed inventions relate generally to lead frame panels suitable for use in packaging semiconductor devices and to packaged semiconductor devices that incorporate a lead frame from such a panel.

One common type of semiconductor package utilizes a thin metal (typically copper) lead frame to form the electrical pins of the package. Figure 1(d) of the present application illustrates several conventional lead frame based packages. In lead frame based packaging, a lead frame strip or panel having a number of device areas thereon is typically used during the manufacturing process so that multiple semiconductor devices can be packaged at the same time.

Figures 1(a) and 1(b) of the present application illustrate a novel lead frame panel that is particularly well suited for forming surface mounted chip scale packages. For convenience of explanation, Figure 1(a) is reproduced below with color coding to help better identify the disclosed components. As seen therein, the lead frame panel 110 has a two dimensional array of device areas. For illustrative purposes, the upper left device area is colored green to highlight the geometry of a single device area. Each device area has a plurality of contacts 112 and a die attach pad 114. The panel has a grid of tie bars 115 (illustrated in red) that extend in perpendicular rows and columns to define the device area. The tie bars 115 carry the contacts 112 and die attach pads 114 (which are illustrated in yellow). The majority of the appealed claims are directed at lead frame panels such as the panel illustrated below.

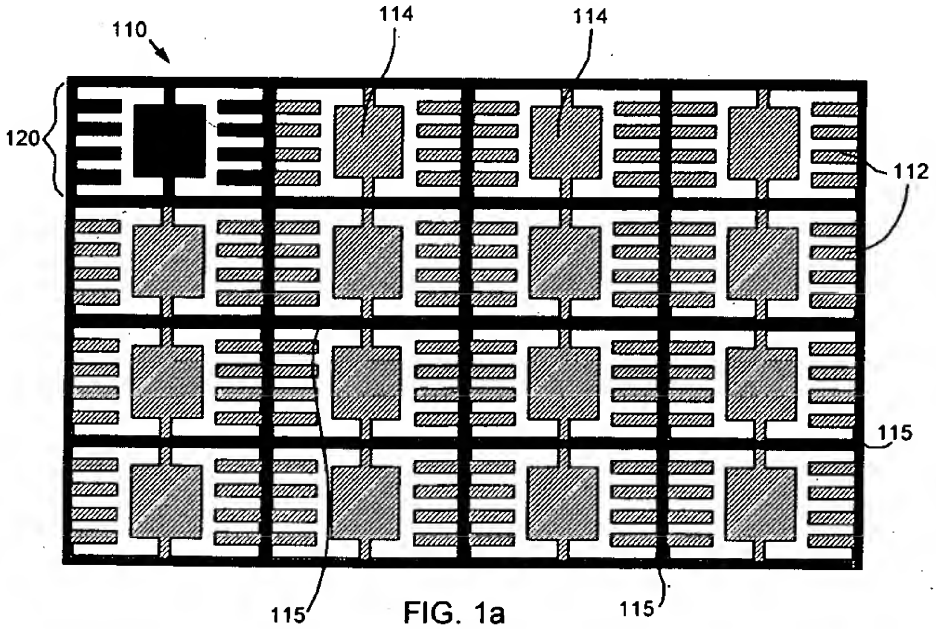

FIG. 1a

As illustrated conceptually in Figures 3(a) and 3(b), during packaging, each die attach pad 114 has an integrated circuit chip 130 (which is often referred to as a "die") mounted thereon. Each integrated circuit chip (die) 130 is then electrically connected to the contacts in its associated device area. In the illustrated embodiments, the electrical connection is accomplished by wire bonding using fine gold wires. This results in a panel structure populated with integrated circuits 130 that are electrically connected to their associated contacts by bonding wires 140 as generally illustrated in Figure 1(b). After the dice have been electrically connected to their contacts, an encapsulant material is dispensed to cover the IC chips 130 and the bonding wires as generally illustrated in Fig. 3(b). In the illustrated embodiment, the encapsulant forms a cap that covers the two dimensional array of device areas, but leaves the bottom surfaces of the contacts 112 exposed to facilitate electrically connecting the package to external devices. Some of the pending claims are generally directed at the populated and encapsulated lead frame panel that exists at this stage of the process.

After encapsulation, the panels may be sawed or otherwise singulated into individual IC packages as generally illustrated in Fig. 3(b). Figure 1(c) illustrates the resulting IC package. A few of the appealed claims are generally directed at the structure of the resulting package.

VI. ISSUES

The issues which applicant believes to be most pertinent to the present appeal include:

(a) Whether the Examiner's characterization of Figs. 1(a)-1(c) of the present application as admitted prior art (AAPA) is proper given that those figures illustrate the inventors own work for which they are unaware of any statutory bars. (All pending claims)

(b) Whether amendments to the specification that merely move the description of selected drawings from one section of the application (the background) to another section of the application (the detailed description) constitutes new matter.

(c) Whether subject matter that is clearly shown in the drawings of an application in a manner that makes it clear that the invention was possessed by the Applicant at the time the application was filed and fully enables those skilled in the art to practice an invention satisfies the requirements of 35 USC 112, 1st paragraph. (Claims 11, 13, 18, 26 and 38).

(d) Whether the art combinations relied on by the Examiner reasonably suggest the use of a cap that covers a two dimensional array of device areas

VII. GROUPING OF CLAIMS

Issue (a) relates to the appropriateness of the primary reference used in all of the outstanding rejections and applies to all of the pending claims. However, the claims do not stand or fall together.

Issue (b) relates to objections to the specification and does not directly relate to the rejection of any of the pending claims.

Issue (c) relates to the 35 USC 112, 1st paragraph rejection of claims 11, 13, 18, 26 and 38. These rejected claims do not stand or fall together and each of the claims will be argued independently.

Issue (d) relates to the art based rejections of claims 22-33 and 38-44. These claims do not stand or fall together. With respect to this issue, claims 22-25 will be argued as one group and claims 26-33 will be argued as a second group and claims 38-44 will be argued as a third group.

VIII. ARGUMENT

1) OVERVIEW OF THE FACTS BEHIND THE ISSUES PRESENTED

Figures 1(a) and 1(b) of the present application illustrate a section of a lead frame panel that the Applicants believe is part of their invention. Figure 1(c) illustrates a single package (out of many) that is made from the lead frame panel illustrated in Fig. 1(a). Applicants believe that this resulting package is also their invention. Unfortunately, Figures 1(a)-1(c) were described in the background section of the application. Therefore, the Examiner has treated the subject matter of Figures 1(a)-1(c) as Applicant's admitted prior art (AAPA). See, e.g., Page 4 of the final office action dated May, 6, 2003. The inventors unequivocally believe that they are the inventors of the subject matter illustrated in Figures 1(a)-1(c) and they are not aware of any disclosures or uses that could constitute prior art under the patent laws. A declaration articulating that belief was filed with Amendment C, which was mailed on January 8th, 2003. A copy of the declaration is attached as Appendix II to this Appeal Brief. Therefore, the inventors have sought to rescind any and all implied and/or express admissions that Figures 1(a)-1(c) constitute prior art. **The alleged AAPA is the sole or primary reference relied on by the Examiner in ALL of the outstanding art based rejections.** See, e.g., Pages 4-6 of the final office action dated May, 6, 2003.

Amendment A mailed April 15th, 2002 sought to move the description of Figures 1(a) –1(c) from the background section of the application to the detailed description section of the application. The Examiner did not originally object to these amendments. See, e.g., the office action dated July 25, 2002. However, in the currently pending Final Office Action, the Examiner has objected to these amendments asserting that they introduce new matter. See, Page 2 of the final office action dated May 6, 2003. The "new matter" objections appears to have two aspects. First, the Examiner appears to assert that moving the description of Figures 1(a)-1(c) from the background section to the detailed description section of the application constitutes new matter. Second, the Examiner asserts that the discussion of the tie bars is new matter.

It is the undersigned's understanding that the Examiner's position is that the description of the subject matter of Figures 1(a)-1(c) in the Background section of the application is an admission of prior art and that any attempt to withdraw such an admission is "new matter" and therefore not permitted. Thus, the primary issues presented relate to whether the description of the inventors own work in the background section of an application constitutes an admission of prior art, and if so,

whether it is possible to rescind such an implied admission when it is clear that the characterization of the subject matter as prior art is in error.

For the reasons set forth below, it is respectfully submitted that as a matter of law, **during prosecution**, an applicant should be and is entitled to rescind an express or implied admission that their own work not subject to a bar of any kind somehow constitutes prior art when it is clear that such a characterization of the work was improper.

It is also respectfully submitted that amendments to the specification that only move the location of subject matter originally disclosed and do not in any way alter the scope or nature of the original disclosure cannot as a matter of law constitute **new matter** even if they effectively remove an improper, implied or express admission of prior art. It is noted that exactly the same issue was addressed in a sister application (US Patent No. 6,589,814 (Serial No. 09/399,585) on substantially the same facts by way of a petition to the commissioner. As articulated in the notice of allowance in the sister application, the decision of the USPTO was to allow entry of the amended figures and text in question.

2) A DISCUSSION OF APPLICANT'S OWN PRIOR WORK CAN NOT BE TREATED AS PRIOR ART IN THE ABSENCE OF A STATUTORY BAR

Section 2129 of the MPEP correctly points out (citing *In re Nomiya*, 184 USPQ 607,610 (CCPA 1975)) that admissions by applicant may generally be treated as prior art. However, the undersigned is not aware of anything in the MPEP or in the case law that suggests that an Applicant cannot correct an improper characterization of the Applicant's own earlier work as "prior art." Rather as pointed out further on in MPEP section 2129 (citing *Reading & Bates*[1]): **"[a]n applicant's own foundational work should not, unless there is a statutory bar, be treated as prior art solely because knowledge of this work is admitted."**[2] Like in *Reading & Bates*, "*Nomiya* is distinguishable from the case at hand, on the same basis *Fout* was distinguished from *Ehrreich* – the

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1 *Reading & Bates Construction Co. v. Baker Energy*, 223 USPQ 1168 (Fed. Cir. 1168).

2 See MPEP section 2129.

existence of a common inventive entity as both the applicant for patent and the inventor of the alleged 'prior art'."[3]

In re Nomiya and many other cases have dealt with situations where an inventor described certain activities *of others* that were known to the inventors before their own invention of the subject matter of the applicant as prior art. Under the law at the time, it was clear that such prior knowledge should be treated as prior art and the applicants never argued that they had not received the information from others prior to their own invention. (It is believed that the art at issue in *Nomiya* would have been prior art under the principle that is 35 USC 102(f) today). This is a very different scenario than the present case. Specifically, in the present case, the background section of the originally filed application described a lead frame and package design (illustrated in Figs. 1(a)-1(c)) **that was the inventors' own work.**[4] It is respectfully submitted that in situations where a discussion in the background describes the applicant's own work that is not the subject of any known statutory bar, such a discussion **should not** be treated as an irrevocable admission of prior art.

It is noteworthy that the relevant drawings (Figs. 1(a)-1(c)) as originally filed WERE NOT labeled as prior art. The inventors have unequivocally stated that the subject matter of Figs 1(a)-1(c) (which is the subject matter that the amendments sought to move from the background to the detailed description portion of the application) is their own work and not, to the best of their knowledge, subject to any statutory bars. Therefore, it is respectfully submitted that any presumption that the subject matter of Figs. 1(a)-1(c) is prior art that may have been implied by discussing this work in the background section of the application or by the language used to discuss the work, has been successfully rebutted by the inventors statements that those figures illustrate their own earlier work and that they are unaware of any events that would cause that work to constitute a statutory bar. So that the record is clear, the Applicants filed a declaration of the inventors confirming that Figs. 1(a) – 1(c) illustrate their own work. This declaration was filed with Amendment C, which was mailed on January 8th, 2003. A copy of that Declaration is attached as Appendix II to this Appeal Brief.

Since the subject matter of Figs. 1(a)-1(c) illustrate the inventors' own work, it is respectfully submitted that they may, as a matter of right, eliminate any inference in the application that such work is somehow prior art to them and that the elimination of such an inference does not in any way constitute new matter as asserted by the Examiner.

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[3] *Reading & Bates Construction Co. v. Baker Energy*, 223 USPQ 1168, 1172 (Fed. Cir. 1168). The cites for the referenced Fout and Ehrreich cases are: *In re Ehrreich*, 200 USPQ 504 (CCPA 1979) and *In re Fouts*, 213 USPQ 532 (CCPA 1982).

[4] See copy of the Declaration of the inventors that is attached as Appendix II to this appeal brief. This Declaration was originally filed with Amendment C which was mailed on January 8th, 2003.

3) THE OUTSTANDING ART BASED REJECTIONS ARE ALL IMPROPER BECAUSE THEY RELY ON ART THAT IS NOT VALID PRIOR ART AGAINST THE PRESENT INVENTIONS.

All of the pending art based rejections are based primarily on the alleged Applicant's admitted prior art. More specifically, the final rejection dated May 6, 2003 organizes the art based rejection of the claims into three groups. First, claims 11-12, 18-33 and 38-44 were rejected as being obvious in view of the alleged AAPA standing alone.[5] Second, claims 13, 15-17, 21, 25, 30 and 38-44 were rejected as being unpatentable over the alleged AAPA in view of Lin's U.S. Patent Nos. 5,200,362 and 5,273,938.[6] Third, the second set of claims (i.e., claims 13, 15-17, 21, 25, 30 and 38-44) were independently rejected as being unpatentable over the alleged AAPA in view of Hur et. al.[7] The specific subject matter that the Examiner alleges is admitted prior art and relies upon in each of these rejections is articulated as the subject matter described at pages 1-3 and illustrated in Figs. 1(a) – 1(d) of the present application.

Initially, as discussed above, the subject matter of Figs. 1(a)-1(c) is NOT prior art. Rather, it is believed to portray a part of Applicant's invention.

It is acknowledged that Figure 1(d) and the corresponding description of those specific figures in the specification IS indeed prior art. However, Figure 1(d) does not disclose or reasonably suggest any of the claimed invention. Although the Examiner has identified Fig. 1(d) in the rejection, it is believed by the undersigned that she is relying exclusively on the subject matter of Figs. 1(a) – 1(c) and the corresponding text in the outstanding rejections. This is in part because Fig. 1(d) does not illustrate any lead frame panels whatsoever, or any devices with contacts or a die attach pad exposed on the bottom surface of the package. Rather, they illustrate conventional lead frame based package designs. If our understanding in incorrect, the Examiner is respectfully requested to articulate the specific parts of Fig. 1(d) or the corresponding description that she is relying on in her Examiner's Answer.

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5 See page 4 of the final office action dated May 6, 2003.
6 See page 5 of the final office action dated May 6, 2003.
7 See page 6 of the final office action dated May 6, 2003.

Since the outstanding rejections are all premised primarily on an improper characterization of the inventors own work as illustrated in Figs. 1(a) – 1(c) as prior art, it is respectfully submitted that **all** of the art base rejections should be reversed for at least this reason.

It is noted that the second and third groups of rejections (i.e., the rejections of claims 13, 15-17, 21, 25, 30 and 38-44), introduced secondary references. However, the Examiner has not alleged that the secondary references standing alone would render any of claims 13, 15-17, 21, 25, 30 or 38-44 obvious. That is not surprising since the secondary references standing alone or in combination do not teach or reasonably suggest and of the claimed combinations. Again, if the Examiner disagrees with the Applicants characterization of the rejections, she is respectfully requested to articulate the portions of the secondary references she would rely on to render the various claims obvious.

In view of the fact that all of the outstanding rejections are all premised primarily on an improper characterization of the inventors' own work as prior art, it is respectfully submitted that **all** of the art base rejections should be reversed for at least this reason.

4) THE GROUP MOLDING OF DEVICE AREAS FEATURE

Claims 22 is specifically directed at lead frame panels having dice mounted thereon and a molded cap that covers a two dimensional array of immediately adjacent device areas that are separated only by the tie bars. The outstanding rejection of claim 22 relies only on the allegedly admitted prior art. It is noted, however, that while Figs. 1(a) and 1(b) illustrate a lead frame panel having a two dimensional array of device areas, they do not show how the device areas are encapsulated. It is believed that most lead frame based packages are individually molded. That is, when encapsulating the device areas in most lead frame strips, each device areas is individually molded. It is respectfully submitted that even if one were to assume, *arguendo*, that the lead frame panels of Figs. 1(a)-1(c) were prior art, that would still not suggest the molded cap over a 2-D array of device areas feature of claim 22 since the device areas of Fig. 1(a) could readily be molded individually as appears to be the case in virtually all of the lead frames based art of record. This distinction was pointed out in an interview that occurred with the Examiner and was pointed out in the amendment mailed January 8th, 2003. Yet the pending rejections continue to merely state that the cap is an obvious variation without providing any art whatsoever that teaches or suggests such an arrangement or articulating a reason why such a design would be obvious to a person of ordinary

skill in the art. It is respectfully submitted that the Examiner's failure to find a reference that in the context of the claimed invention (e.g. a panel suitable for forming leadless leadframe type packages) utilizes a cap that encapsulates a 2-D array of device areas is strong evidence that the use of such an integrated cap is non-obvious. Accordingly, it is respectfully submitted that the outstanding rejection of claim 22, as well as claims 23-24, which depend from claim 22, should be reversed for this reason as well.

Independent Claim 26 is also directed at panel assemblies suitable for use in packaging a 2-D array of integrated circuits simultaneously. The panel assembly includes a lead frame panel patterned to define at least one two dimensional array of adjacent device areas that are each suitable for use as part of an independent integrated circuit package. This claim further requires a molded cap that covers the array of device areas, while leaving the bottom surfaces of the contacts exposed. The outstanding rejection of claim 26 is also based solely on the alleged AAPA standing alone. As pointed out above, even if Figures 1(a) – 1(c) were prior art, they do not suggest either the use of a molded cap that covers a 2-D array of device areas or the exposure of the bottom contacts of the lead frame. Accordingly, it is respectfully submitted that the outstanding rejection of claim 26, as well as claims 27-29 and 31-33 which depend from claim 26 should be reversed for this reason as well.

Claims 38-44 are also directed at panel assemblies suitable for use in packaging a 2-D array of integrated circuits simultaneously. The panel assembly includes a lead frame panel patterned to define at least one two dimensional array of adjacent device areas that are each suitable for use as part of an independent integrated circuit package. Like claim 26, these claims also require a molded cap that covers the array of device areas, while leaving the bottom surfaces of the contacts exposed. These claims were rejected on the basis of the alleged AAPA standing alone or in combination with various secondary references. As pointed out above, the alleged AAPA does not teach or suggest either the use of a molded cap that covers a 2-D array of device areas or the exposure of the bottom surfaces of the contacts. Additionally, none of the secondary references teach or suggest these features. Accordingly, it is respectfully submitted that the outstanding rejections of claim 38-44 should be reversed for this reason as well.

Claims 25 and 30 depend from claims 22 and 26 respectively and were rejected on the basis of the alleged AAPA in combination with various secondary references. Again, neither the alleged AAPA or the secondary references teach the features of claims 22 and 26. Accordingly, it is respectfully submitted that the outstanding rejections of claims 25 and 30 should be reversed for the same reasons as their respective base claims.

5) THE MOVEMENT OF TEXT FROM ONE PART OF AN APPLICATION (THE BACKGROUND) TO ANOTHER PART OF AN APPLICATION (THE DETAILED DESRIPTION) CANNOT BE CONSIDERED THE INTRODUCTION OF NEW MATTER.

As indicated above, the amendments to the specification that have been objected to by the Examiner primarily move the description of Figs. 1(a) – 1(c) from the background section to their proper location in the detailed description section of the application. The Examiner appears to be taking the position that the movement of the description of Figs. 1(a) – 1(c) to the detailed description section of the application somehow constitutes new matter. It is believed that this is in direct conflict with PTO policy. Specifically, Section 2163.06 of the MPEP states (first paragraph, third sentences) **"information contained in any one of the specification, claims or drawings of the application *as filed* may be added to *any other part* of the application *without* introducing new matter."** Accordingly, it is respectfully submitted that the outstanding objections to the amendment under 35 USC 132 should be reversed for at least this reason. More specifically, it is respectfully submitted that moving the,description of Figs. 1(a)-1(c) from the background section of the application to the detailed description should not be treated as new matter, in line with the practice set out in the MPEP as quoted above, and that the Examiner's pending objection to the specification should be reversed. Moreover, as explained above, an Applicant's own work that is not subject to a statutory bar cannot be construed as prior art. Therefore, it is respectfully submitted that the Examiner's suggestion that amendments making it clear that the subject matter of Figs. 1(a) – 1(c) is not prior art somehow constitutes new matter is groundless.

6) THE DESCRIPTION AND LABELING OF THE TIE BARS DOES CONSTITUTE NEW MATTER.

The Examiner appears to assert that Applicants' mere labeling of the tie bars 115 in certain existing figures (i.e., Figs. 1(a) and 1(b)) as well as their brief description in the amendments to the specification constitutes new matter. Initially, we discuss the assertion that the mere labeling of tie bars that were prominently illustrated in the original drawings somehow constitutes new matter. The proposed amendments to the drawings did not make any changes to Figures 1(a) and 1(b) whatsoever. They merely labeled features such as the tie bars 115 that were very clearly shown in the drawings as originally filed. Since no new features were shown in the drawing, it is respectfully

submitted that as a matter of law, the labeling of preexisting features that were clearly shown cannot in any way constitute new matter. Accordingly, it is respectfully submitted that the Examiner's objection to the labeling of the tie bars should be reversed for at least this reason.

The Examiner has also taken the position that the description of the ties bars provided in the amendment to the specification may constitute new matter. In the outstanding objection, the Examiner does not point to any particular language as being inappropriate. Rather, she appears to have suggested that any mention of the tie bars necessarily constitutes new matter. This is respectfully traversed. By way of background, the only mention of the tie bars in the proposed amendments is the following:

> Referring again to Figs. 1a, panel 110 includes a two dimensional array of device areas. Each device area has a plurality of contacts 112 and a die attach pad 114. **The panel has a grid of tie bars 115 that extend in perpendicular rows and columns to device the device areas. The tie bars 115 carry the contacts 112 and die attach pads 114.**

It is respectfully submitted that the brief mention of the tie bars 115 quoted above merely describes the geometric arrangement that can be clearly seen in Figs. 1(a) and 1(b) and thus does not in any way constitute new matter. Specifically, the horizontal and vertical elements that run the width and height of the lead frames of Figures 1(a), 1(b), 2(a) and 2(b) are "bars" that "tie" the die attach pads 114 and surrounding contacts 112 together. The term "tie bars" is therefore wholly appropriate and would readily be recognized by one of ordinary skill in the art from even a cursory review of the figures. In view of the foregoing, it is respectfully submitted that the Examiner's objection to the portions of the amendments that describe the tie bars should be reversed.

For the convenience of review, Figure 1(a) is reproduced again below with color coding to help better identify the illustrated components. It is noted that some of the number labels are new. As seen in the figure, the lead frame panel 110 has a two dimensional array of device areas. For illustrative purposes, the upper left device area is colored green to highlight the geometry of a single device area. Each device area has a plurality of contacts 112 and a die attach pad 114. The panel has a grid of tie bars 115 (illustrated in red) that extend in perpendicular rows and columns to define the device area. The tie bars 115 carry the contacts 112 and die attach pads 114 (which are illustrated in yellow). Again, it is respectfully submitted that the original drawings clearly show the tie bars 115.

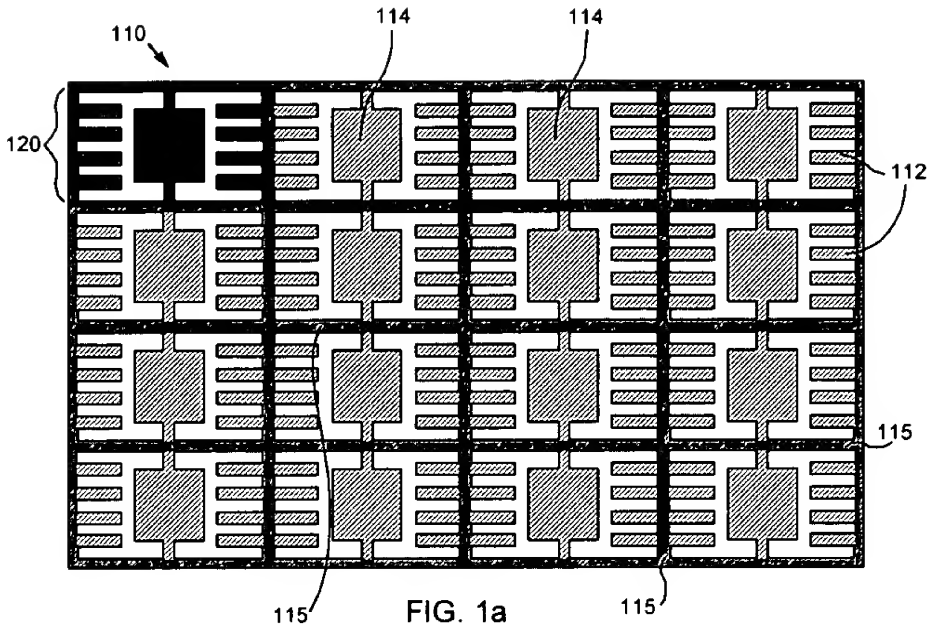


FIG. 1a

7) THE SUBJECT MATTER OF CLAIMS 11, 13, 18, 26 AND 38 IS FULLY DISCLOSED IN THE SPECIFICATION

The Examiner rejected claims 11, 13, 18, 26 and 38 (each of the independent claims) under 35 USC 112, first paragraph as not having been described in the specification as originally filed. See, page 3 of final office action dated May 6th, 2003. Specifically, the Examiner appears to object to the language relating to the formation of: "an array," a "matrix," a "two-dimensional array of components" and/or the tie bars. Initially, it is noted that the Examiner appears to be attempting to make a written description type rejection. She does not appear to be arguing that the claims are not enabled by the specification. However, the Examiner has not clearly articulated the basis for her rejection of the claims. MPEP §2163 articulates the guidelines for Examining applications under the written description requirement. MPEP §2163.04 requires that in rejecting a claim under the written description requirement, the Examiner must set forth express findings of fact which support the lack of written description conclusion.

> These finding should:
>
> (A) Identify the claim limitation at issue; and
>
> (B) Establish a *prima facia* case by providing reasons why a person skilled in the art at the time the application was filed would not have recognized that the inventor was in possession of the invention as claimed in view of the disclosure of the application as filed. *See MPEP §2163.04.*

In the present case, the Examiner has failed to do either. That is not surprising because as can be clearly seen in the figure above, the broad language objected to is merely a simple explanation of the geometry of the lead frame panel clearly illustrated in Figs. 1(a), 1(b), 2(a) and 2(b). Thus, it is clear from the specification as originally filed that the inventors were in full possession of the currently claimed inventions at the time the present application was filed.

More particularly, as can be clearly seen in Fig. 1(a) reproduced above (or any of the other figures), the lead frame panel 110 has a two dimensional array of device areas 120. (As pointed out above, a single one of the device areas is colored green in the reproduction of Fig. 1(a) above). In the illustrated embodiment, the components within each device area are clearly shown as being tied together by tie bars 115 that are arranged in a matrix. Therefore, it is respectfully submitted that the application as originally filed fully disclosed the subject matter set forth in all of the rejected claims. It is noted that the amendments that have been recently objected to by the Examiner include a short explanation of the structure of Fig. 1(a) that is believed to articulate what would be readily apparent to anyone of ordinary skill in the art that reviews that figure.

The Examiner has not pointed out specific claim language that she believes to be unsupported by the original disclosure. In claim 11, it is suspected that the only language objected to is the recitation: "an array of device areas" that appears in the last line (line 16) of the claim. It is respectfully submitted that an array of device areas is clearly shown in all of Figs. 1(a), 1(b), 2(a) and 2(b) of the originally filed application. Accordingly, it is respectfully submitted that the rejection of claim 11 under 35 USC 112 1st paragraph should be reversed for at least this reason.

In claim 13, it is suspected that the only language objected to is the recitation: "said lead frame comprising a two dimensional array of die attach pads and conductive leads" that appears at lines 18-19 of the claim. It is respectfully submitted that this arrangement of the die attach pads 114 and contacts 112 is clearly shown in all of Figs. 1(a), 1(b), 2(a) and 2(b) of the originally filed application. Accordingly, it is respectfully submitted that the rejection of claim 13 under 35 USC 112 1st paragraph should be reversed for at least this reason.

In claim 18, it is suspected that the language objected to is the recitation: "a matrix of tie bars that extend in substantially perpendicular rows and columns to define a two dimensional array of immediately adjacent device areas separated only by the tie bars." This language appears at lines 4-6 of the claim. It is respectfully submitted that this arrangement of the tie bars 115 that defines a two dimensional array of device areas is clearly shown in all of Figs. 1(a), 1(b), 2(a) and 2(b) of the

originally filed application. Accordingly, it is respectfully submitted that the rejection of claim 18 under 35 USC 112 1st paragraph should be reversed for at least this reason.

In claim 26, it is suspected that the language objected to is the recitation: "the lead frame panel being patterned to define at least one two dimensional array of adjacent device areas." This language appears at lines 3-4 of the claim. It is respectfully submitted that this arrangement of the lead frame panel having a two dimensional array of adjacent device areas is clearly shown in all of Figs. 1(a), 1(b), 2(a) and 2(b) of the originally filed application. Accordingly, it is respectfully submitted that the rejection of claim 26 under 35 USC 112 1st paragraph should be reversed for at least this reason.

In claim 38, it is suspected that the language objected to is the recitation: "the lead frame panel being patterned to define at least one two dimensional array of adjacent device areas." This language appears at lines 3-4 of the claim and is the same as the language quoted above for claim 26. Again, it is respectfully submitted that this arrangement of the lead frame panel having a two dimensional array of adjacent device areas is clearly shown in all of Figs. 1(a), 1(b), 2(a) and 2(b) of the originally filed application. Accordingly, it is respectfully submitted that the rejection of claim 38 under 35 USC 112 1st paragraph should be reversed for at least this reason.

In the outstanding 112 rejection, the Examiner also objected to the language relating to a "rectangular footprint perpendicular to a bottom surface" and the "formation of sharp corners." See, page 3 of final office action dated May 6th, 2003. It is believed that such language does not appear in any of the pending claims. (Rather such language appeared in claims that have been cancelled). Therefore, we do not address these objections. If the Examiner believes that objectionable language to this effect is in any of the pending claims, she is respectfully requested to point it out in the Examiner's Answer.

8) COMMENTS RE THE PARENT APPLICATION

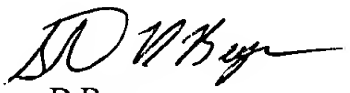
At page 2 of the outstanding office action, the Examiner comments that this application is a divisional of 09/054,422 (which is now US Patent No. 6,130,473). The status of the parent patent is not believed to be particularly relevant to the present application. However, for completeness, it is noted that a reissue application has been filed in the parent patent in order to introduce amendments

to the specification that move the discussion of Figures 1(a)- 1(c) from the background section of the application to the detailed description portion of the application. It is also noted that Figures 1(a)-1(c) are NOT labeled as Prior Art in the issued patent.

9) CONCLUSION

In view of the forgoing, it is respectfully submitted that the subject matter of Figs. 1(a) – 1(c) is not prior art to the present application and that all of the pending rejections should be reversed for at least this reason. It is also respectfully submitted that the Examiner's objections to the amendment filed 4-26-2002 are improper and should also be reversed. Additionally, it is respectfully submitted that the Examiner's rejection of claims 11, 13, 18, 26 and 38 under 35 USC 112, first paragraph is improper and should be reversed.

Respectfully Submitted,
BEYER WEAVER & THOMAS



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VII. APPENDIX I

CLAIMS ON APPEAL

11. A lead frame panel suitable for forming an array of integrated circuit packages for accommodating a semiconductor die, the lead frame panel having an array of device areas, each device area being suitable for forming an independent integrated circuit package and comprising:

a planar lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads, wherein the plastic encapsulation is part of a molded cap that covers an array of the device areas.

12. An integrated circuit package as in Claim 11, further comprising a solder ball attached to each of said exposed lower surface of said conductive leads.

13. An integrated circuit package for accommodating a semiconductor die, comprising:

a planar lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around

an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads; and

an adhesive pad removably attached to said integrated circuit package, covering said lower surface of said die attach pad and said lower surfaces of said conductive leads, and

wherein said integrated circuit package is one of a plurality of integrated circuit packages fabricated simultaneously on said lead frame, said lead frame comprising a two dimensional array of die attach pads and conductive leads that are positioned under the plastic encapsulation, and wherein said adhesive pad supports the array of die attach pads and conductive leads prior to singulation of the plurality of integrated circuit packages.

15. An integrated circuit package as in Claim 13, wherein said lead frame is fabricated on a metal panel.

16. An integrated circuit package for accommodating a semiconductor die, comprising:

a planar lead frame fabricated on a metal panel comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads; and

an adhesive pad removably attached to said integrated circuit package, covering said lower surface of said die attach pad and said lower surfaces of said conductive leads,

wherein said integrated circuit package is one of a plurality of integrated circuit packages fabricated simultaneously from said lead frame, said lead frame comprising an array of die attach pads and conductive leads, and said adhesive pad supports said die attach pads and said conductive leads prior to singulation of said plurality of integrated circuit packages and

further comprising an encapsulant dam provided to enclose said array of die attach pads and conductive leads.

17. An integrated circuit package as in Claim 13, wherein said array of die attach pads and conductive dies is being arranged in a regular pattern so as to allow singulation of said integrated circuit packages by sawing through said plastic encapsulation and said conductive leads at predetermined positions.

18. A lead frame panel suitable for use in packaging an array of integrated circuits, the lead frame panel being formed from a conductive sheet and having top and bottom surfaces, the lead frame panel comprising:

a matrix of tie bars that extend in substantially perpendicular rows and columns to define a two dimensional array of immediately adjacent device areas separated only by the tie bars, each device area being suitable for use in an independent integrated circuit package;

a multiplicity of die attach pads; and

a multiplicity of conductive contacts, the conductive contacts being mechanically carried by the tie bars; and

wherein each device area includes one of the die attach pads and a plurality of the conductive contacts that are positioned generally adjacent the die attach pad.

19. A lead frame panel as recited in claim 18 wherein the die attach pads, the conductive contacts and the tie bars are all substantially co-planar.

20. A lead frame panel as recited in claim 19 wherein the conductive contacts and the die attach pads are substantially the same thickness.

21. A lead frame panel as recited in claim 18 further comprising an adhesive tape adhered to a bottom surface of the lead frame panel.

22. A panel assembly of integrated circuits comprising:

a lead frame panel as recited in claim 18;

a plurality of dice, each die being carried by an associated die attach pad; and

a molded cap that covers the array of device areas while leaving bottom surfaces of the die attach pads and the conductive contacts exposed, wherein encapsulation material that forms the molded cap is exposed at a bottom surface of the panel assembly.

23. A packaged integrated circuit formed by singulating the panel assembly recited in claim 22, wherein the conductive contacts in the packaged integrated circuit do not extend beyond the edge of the encapsulation material in the packaged integrated circuit and the die attach pad in the packaged integrated circuit is exposed.

24. A packaged integrated circuit as recited in claim 23 wherein the conductive contacts and the die attach pad are substantially the same thickness.

25. A panel assembly as recited in claim 22 further comprising an adhesive tape adhered to a bottom surface of the lead frame panel, whereby the adhesive tape serves to keep the exposed surface of the exposed encapsulation material substantially co-planar with the bottom surfaces of the contacts and die attach pads.

26. A panel assembly suitable for use in packaging an array of integrated circuits simultaneously, the panel assembly having top and bottom surfaces and comprising:

a lead frame panel formed from a conductive sheet, the lead frame panel being patterned to define at least one two dimensional array of adjacent device areas, each device area being suitable

for use as part of an independent integrated circuit package and including a die and a plurality of contacts positioned around and electrically connected to the die; and

a molded cap that substantially uniformly covers the array of device areas while leaving bottom surfaces of the conductive contacts exposed to facilitate electrical connection to external components, wherein encapsulation material that forms the molded cap is exposed at a bottom surface of the panel of integrated circuits to physically isolate the contacts.

27. A panel assembly as recited in claim 26 wherein:

each device area in the lead frame panel further includes a die attach pad; and

bottom surfaces of the die attach pads are also exposed.

28. A panel assembly as recited in claim 27 wherein the die attach pads, the conductive contacts and the tie bars are all substantially co-planar.

29. A panel assembly as recited in claim 28 wherein the conductive contacts and the die attach pads are substantially the same thickness.

30. A panel assembly as recited in claim 26 further comprising an adhesive tape adhered to a bottom surface of the lead frame panel, whereby the adhesive tape serves to keep the encapsulation material exposed at the bottom of the panel assembly substantially co-planar with the bottom surfaces of the contacts and die attach pads.

31. A panel assembly as recited in claim 26 further comprising bonding wires for electrically coupling the dice to their associated contacts, wherein the molded cap encapsulates the bonding wires.

32. A packaged integrated circuit formed by singulating the panel assembly recited in claim 26, wherein the conductive contacts in the packaged integrated circuit do not extend beyond the edge of the encapsulation material that is part of the packaged integrated circuit.

33. A packaged integrated circuit as recited in claim 32 wherein the integrated circuit is singulated by sawing the panel assembly along substantially perpendicular lines.

38. A panel assembly suitable for use in packaging an array of integrated circuits, the panel assembly having top and bottom surfaces and comprising:

a lead frame panel formed from a conductive sheet, the lead frame panel being patterned to define at least one two dimensional array of adjacent device areas, each device area being suitable for use as part of an independent integrated circuit package and including a plurality of contacts;

a plurality of dice, each die being associated with one of the device areas and being electrically connected to the associated contacts; and

a molded cap that covers the array of device areas while leaving bottom surfaces of the contacts exposed to facilitate electrical connection to external components, wherein encapsulation material that forms the molded cap is exposed at a bottom surface of the panel of integrated circuits to physically isolate the contacts; and

an adhesive pad adhered to a bottom surface of the lead frame panel, whereby the adhesive pad serves to keep the encapsulation material exposed at the bottom of the panel assembly substantially co-planar with the bottom surfaces of the contacts and die attach pads.

39. A panel assembly as recited in claim 38 wherein:

each device area in the lead frame panel further includes a die attach pad; and

bottom surfaces of the die attach pads are also exposed.

40. A panel assembly as recited in claim 39 wherein the lead frame panel further comprises tie bars that support the contact, wherein the device areas are substantially immediately adjacent one another with only the tie bars residing therebetween.

41. A panel assembly as recited in claim 40 wherein the die attach pads, the contacts and tie bars are all substantially co-planar.

42. A panel assembly as recited in 39 wherein the conductive contacts and the die attach pads are substantially the same thickness.

43. A panel assembly as recited in claim 38 further comprising bonding wires for electrically coupling the dice to their associated contacts, wherein the molded cap encapsulates the bonding wires.

44. A packaged integrated circuit formed by singulating the panel assembly recited in claim 38, wherein the contacts in the packaged integrated circuit do not extend beyond the edge of the encapsulation material that is part of the packaged integrated circuit.